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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,498	04/13/2004	Anton Kotz	CREM-00101-UUS	3283
33794	7590	08/23/2006	EXAMINER	
MATTHIAS SCHOLL 14781 MEMORIAL DRIVE SUITE 1319 HOUSTON, TX 77079				SIDDIQUI, SAQIB JAVAID
		ART UNIT		PAPER NUMBER
		2138		

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/823,498	KOTZ ET AL.
	Examiner Saqib J. Siddiqui	Art Unit 2138

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 June 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-22 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-22 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 13 April 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>9/20/04, 7/02/04, 06/29/04</u> | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Priority

Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in Application No. 10/823498, filed on June 30, 2004.

Oath/Declaration

The Oath filed June 30, 2004 complies with all the requirements set forth in MPEP 602 and therefore is accepted.

Drawings

The filed drawings are accepted.

Specification

The contents of the filed specification are accepted.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 7, 14:

The phrase "in particular" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

The phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

The phrase "matrix-like" renders the claim(s) indefinite because the claim(s) include(s) elements not actually disclosed (those encompassed by "or the like"), thereby rendering the scope of the claim(s) unascertainable. See MPEP § 2173.05(d).

As per claims 2, 10, & 15:

The phrase "at least partial information with respect to" renders the claim indefinite because it is unclear in what way the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d). For the purposes of compact prosecution the examiner assumes that the libraries contain information regarding at least one of the specifics from the list.

As per claims 3, 9, & 17:

These claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant mentions that each "dimension" holds a different set of data. However, it is unclear to understand how one dimension can hold a certain value without intersecting the other dimension, since in matrices each data value's position is denoted by at least two dimensions (row, column). For the purposes

of compact prosecution the examiner assumes that the multidimensional matrix is a central database with different values stored in a pattern.

As per claims 5, 12, & 19:

These claims are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The applicant claims "generally legible manner", it is unclear what applicant means by "generally legible", further examiner would like to point out that the sentence structure of these claims makes it extremely difficult for the examiner to clearly understand the limitations of these claims. Appropriate correction is requested.

As per claims 6, 13, & 16:

The phrase "for example" renders the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

The phrase "such as" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

The phrase "preferably" renders the claim indefinite because it is unclear whether the limitations following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

As per claims 8, 11,18, & 20-22:

These claims are rejected by virtue of their dependency. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, 29-33, and 37 are rejected under 35 U.S.C. 102 (b) as being fully anticipated by Peters et al. US Pat no. 4,606,025.

As per claim 1:

Peter et al. teaches a method which generates an IC tester control consisting of numerous test instructions for a plurality of specific test environments, which can generate and measure analog and digital signals for an IC, in particular a mixed-signal IC (column 2, lines 35-67), wherein the method obtains data and control instructions from multidimensional test matrices independent of the test environment, such as matrix-like databases or libraries (Figure 1 # 12, column 4, lines 19-40), the data and control instructions independent of the test environment are converted by means of a code generator into a syntax which is dependent on the test environment and which can be integrated into a general syntax dependent on the test environment (Figure 1 # 14 & 16), so that the syntax dependent on the test environment and the general syntax dependent on the test environment together form a complete control, comprising analog and digital signals, for one of the specific test environments (Figure 1 # 19A-X).

As per claim 2:

Peter et al. teaches a method as rejected in claim 1 above, wherein, during its conversion phase, the code generator employs a library group in which are integrated various libraries which contain at least partial information with respect to a) the test environment (Figure 1 # 20A), b) the syntax dependent on the test environment, c) the test environment resources, d) the sequence of test methods, e) the standard functions of the test environment, f) the load board structure, g) the standard functions dependent on the load board and h) the code generator optimization.

As per claim 3:

Peter et al. teaches a method as rejected in claim 1 above, wherein a multidimensional test matrix has, in a first dimension, data on the number and arrangement of pins of the IC, in a further dimension, data on the meaning, the name and the signal flow direction of the pins of the IC, in a further dimension, sequences of test instructions, in a further dimension, test instruction headings which summarize individual test instructions, in one dimension, specifies general test conditions, in one dimension, specifies the start conditions for a test, in one dimension, specifies test patterns, in one dimension, specifies functional descriptions of the tests, in one dimension, specifies switching values, in one dimension, specifies conditions for quality sorting of ICs. (Figures 3A-L).

As per claim 5:

Peter et al. teaches the method as rejected in claim 1 above, wherein a processible data sheet of the IC serves as the origin for the matrices independent of the test environment, on the basis of which data sheet automated test description

documentations are generated from the matrices and name, in a generally legible manner, the scope, the type, the duration and the type of the data and control instructions (Figure 1 # 12).

As per claim 6:

Peter et al. teaches the method as rejected in claim 1 above, wherein signals which are analog and/or digital are read in from the test environment (columns 7-8), preferably with a time lag after superposition of signals of the control, in order to be evaluated via mixed-signal test methods, such as, for example, a method for the gain or gains, the voltage ratios, the frequency responses, the phase positions, the wave shapes, the harmonics and/or the transit-time behavior.

As per claim 7:

Peter et al. teaches a method which generates an IC tester control, consisting of numerous test instructions, for a plurality of specific test environments, which can generate and measure analog and digital signals for an IC, in particular a mixed-signal IC (column 2, lines 35-67), wherein the individual specific test environments differ from one another in their structure and/or their syntax (Figure 1 # 21A-X), the method obtains data and control instructions from multidimensional test matrices independent of the test environment, such as matrix-like databases or libraries (Figure 1 # 12, column 4, lines 19-40), the data and control instructions independent of the tester environment are converted by means of a code generator into a syntax which is dependent on the test environment and which can be integrated into a general syntax dependent on the test environment (Figure 1 # 14 & 16), so that the syntax dependent on the test environment

and the general syntax dependent on the test environment together form a complete control, comprising analog and digital signals, for one of the specific test environments (Figure 1 # 19A-X).

As per claim 8:

Peter et al. teaches the method as rejected in claim 7 above, wherein, in the multidimensional test matrices, it is possible to list test methods which enable both digital and analog signals of the control of the test environment to occur synchronously (columns 7-8).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 4 are rejected under 35 U.S.C. 103(a) as being unpatentable in view of Peters et al. US Pat no. 4,606,025.

As per claims 4:

Peter et al. substantially teaches a method as rejected in claim 1 above, wherein the code generator comprises at least one of the following components; a DC test generator which reads out and converts the data and control instructions from matrices (Figure 6), which generate DC voltage values for an IC in the test environment, an AC test generator which reads out and converts the data and control instructions from matrices, which generate AC voltage values or signal curves for an IC in the test environment (Figure 7), a digital test generator which reads out and converts the data and control instructions from matrices, which generate digital voltage values for an IC in the test environment, a load board generator which reads out and converts the data and control instructions from matrices, which refer to the resources and requirements with respect to the load conditions of the load boards of the test environment, a test rule verifier which checks whether the data and control instructions of the syntax dependent on the test environment can be executed in the test environment, and the code generator runs through a multistage method in the first stage of which the data and control instructions of a matrix are made available to the code generator as source information column (column 4, lines 20-45), in the second stage of which the source information is processed in succession, in each case by one of the components (columns 4-5), the last component being the test rule verifier.

Peter et al. does not explicitly teach optimizing the instructions. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to optimize the instructions, since it has been held that where the general conditions of

a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As per claims 9-13:

These claims teach the same limitations as claims 1-8, and hence the grounds of rejection stay the same.

As per claims 14-22:

Claims 14-22 are directed to the method of the method of claims 1-8. Peter et al. teaches as stated above, the method as set forth in claims 1-8. Therefore, Peter et al. also teaches as stated above, the a method as set forth in claims 14-22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30.

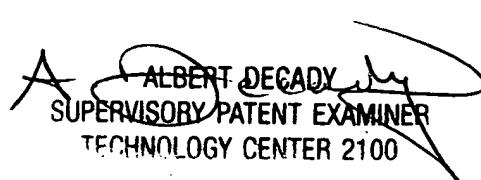
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decay can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Examiner's Note: Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings in the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant, in preparing the responses, to fully consider the references in entirety as potentially teaching all or part

of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the examiner

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

S.S
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08/09/2006


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